

WHAT IS CLAIMED IS:

1. 1. A system for transferring data from an incoming source to an outgoing destination, the system comprising:
- a buffer storage coupled to the incoming source for receiving and storing data from the incoming source;
- a buffer storage address generator for sequentially addressing the buffer storage so that incoming data is stored sequentially within the buffer storage;
- address storage including one or more addresses for accessing the buffer storage;
- an address storage address generator for sequentially accessing the one or more addresses stored in the address storage; and
- an output stage, wherein the output stage retrieves data from the buffer storage in accordance with the one or more addresses accessed by the address generator.
2. The system of claim 1, wherein the data is telephony data.
3. The system of claim 2, wherein the incoming data is organized into timeslots, wherein the buffer storage is organized so each timeslot corresponds to a unique word location in the buffer storage.
4. The system of claim 3, wherein a word location in the buffer storage is 32 bits in length.
5. The system of claim 4, wherein the addresses include bits, wherein the lower-order two bits of each address are used to identify one of four bytes in a word location in the buffer storage.
6. The system of claim 1, further comprising
- a clock having a clock cycle and outputting a clock signal; and

3                   Wherein the buffer storage and address storage address generators are  
4 coupled to a signal derived from the clock signal so that a word of data is stored into the  
5 buffer storage at the start of each clock cycle and a word of data is read out from the  
6 buffer storage by the end of each clock cycle.

1                   7.       The system of claim 1, wherein four consecutive addresses stored  
2 in the address storage are used to each identify a portion of data from one or more  
3 locations in the buffer storage.

1                   8.       A hardware switching system for routing digital data streams in a  
2 network, the hardware switching system including:

3                               a memory for storing incoming data;

4                               an indirect memory addressing mechanism for accessing incoming  
5 data stored in the memory; and

6                               an output control coupled to the indirect memory addressing  
7 scheme and the indirect memory addressing mechanism for selectively outputting  
8 portions of the data in accordance with the indirect memory addressing mechanism.

1                   9.       A method for switching digital data streams in a network, wherein  
2 the digital data streams include timeslots, the method comprising:

3                               storing the incoming data in a memory in accordance with the  
4 timeslots; and

5                               indirectly accessing the memory to determine which portions of the  
6 data to output.

1                   10.     The method of claim 9, wherein the incoming and output data is  
2 organized into multiple timeslots, the method further comprising:

3                               the step of storing incoming data in a memory including the  
4 substep of assigning memory locations to timeslots so that incoming data in a  
5 predetermined timeslot is stored in a predetermined memory location; and

6 the step of indirectly accessing the memory further comprising the  
7 substeps of:

8 using multiple addresses to access multiple memory  
9 locations wherein only a portion of each memory location is used; and

10 combining the data in the accessed multiple memory  
11 locations to form output data to be assigned to a single timeslot.

1 11. The method of claim 9 stored in a machine-readable medium.

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